USB 3.1

What you need to know

REFERENCE GUIDE

Tektronix®

Content

This quick reference guide provides an overview of key USB 3.1 specifications (rev 1.0 July 23, 2013) and important testing considerations for testing both USB transmitters and receivers.

Benefits of Implementing Type-C

POWER DELIVERY

More **Power** with USB Power Delivery (100W)

TYPE-C

More **Flexibility** with new reversible USB Type-C connector

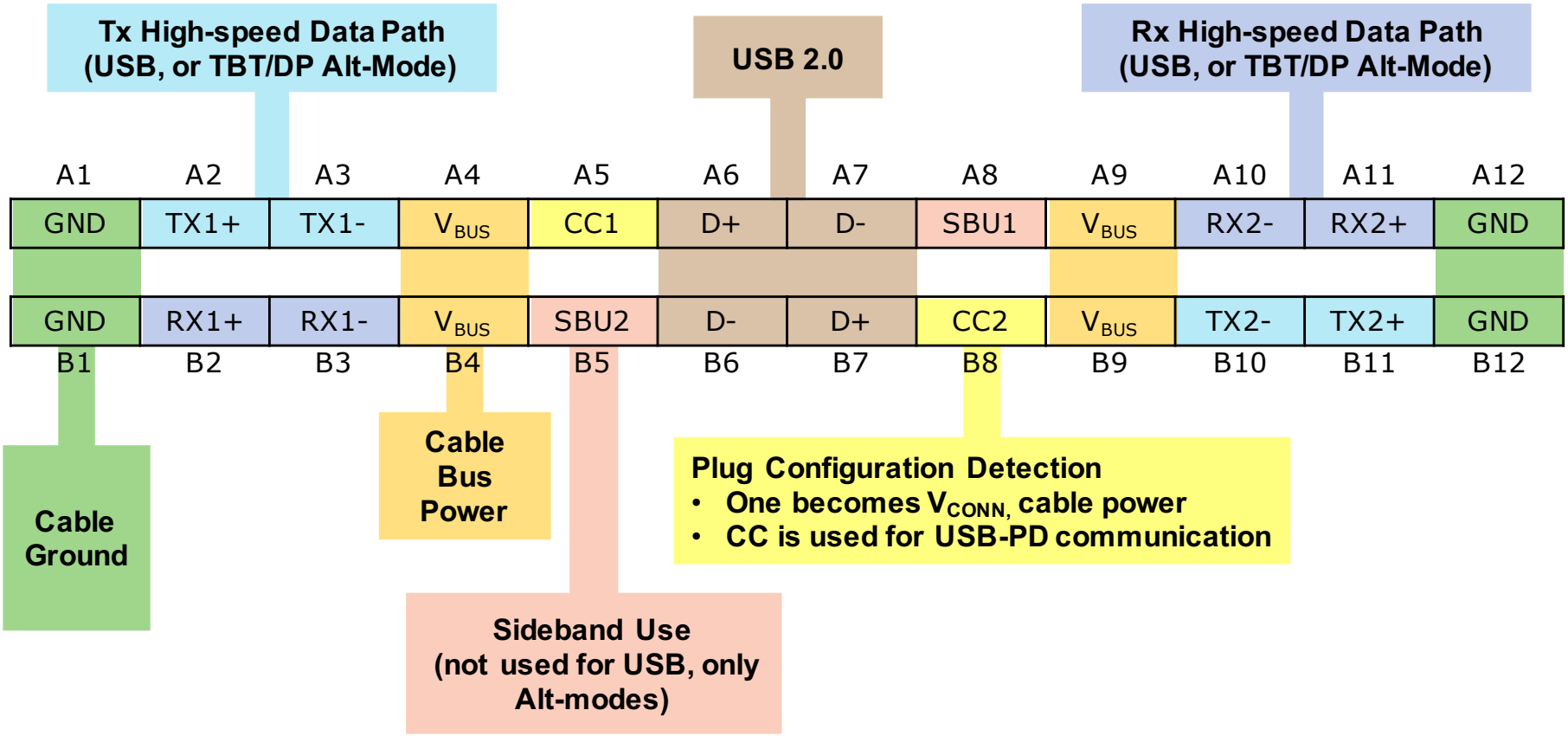
ALTERNATE MODE

More **Protocols** (DisplayPort, Thunderbolt, HDMI, etc.)

USB IF

More **Speed** with USB 3.1 (10 Gbit/s)

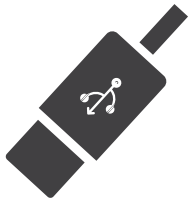
Type-C Pin Definitions



USB 3.1 Generation Comparison

USB 3.1	GEN 1	GEN 2
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	Cable + Host/Device Channels (-20dB, 2.5GHz)	Cable + Board Ref Channels (-23dB, 5GHz)
LTSSm	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	67.1 ps (0.671 UI)
Backwards Compatibility	Yes	Yes
Connector	Std. A, Micro, Type-C	Std. A, Micro, Type-C

USB 3.1 Transmitter Measurement Overview



GEN 1 Overview

GEN 2 Overview

MEASUREMENT	Sigtest v.3.2.11.2	Tektronix DPOJET	Compliance Pattern	Sigtest v4.0.23	Tektronix DPOJET	Compliance Pattern
Jitter Budget (RJ, DJ and TJ)	Yes	Yes	CP0,CP1	Yes	Yes	CP9,CP10
Eye Diagram	Yes	Yes	CP0	Yes	Yes	CP9
Width@BER	Yes	Yes	CP0	Yes	Yes	CP9
Height@BER	-	-	-	No	Yes	CP9
SSC Deviation	No	Yes	CP1	Yes	Yes	CP10
SSC Modulation Rate	No	Yes	CP1	Yes	Yes	CP10
Differential pk-pk Voltage	No	Yes	CP0	No	Yes	CP9
Tx Equalization	-	-	-	Yes	Yes	CP13,14,15
LFPS	Yes	Yes	-	Yes	Yes	-

Data Scrambling

GEN 1 DATA SCRAMBLING OPERATION

The scrambling function is implemented using a **free running Linear Feedback Shift Register (LFSR)**. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding.

On the receive side, descrambling is applied to characters after 8b/10b decoding. The LFSR is reset whenever a COM symbol is sent or received.

The data scrambling rules are as follows:

1. The LFSR implements the polynomial: **G(X)=X16+X5+X4+X3+1**
2. The LFSR value shall be advanced eight serial shifts for each Symbol except for SKP.
3. All 8b/10b D-codes, except those within the Training Sequence Ordered Sets shall be scrambled.
4. K codes shall not be scrambled.

GEN 2 DATA SCRAMBLING OPERATION

The scrambler used for Gen 2 operation is different than the scrambler used for Gen 1 operation. For Gen 2, the LFSR uses the following polynomial: **G(X) = X23 + X21 + X16 + X8 + X5 + X2 + 1**.

The scrambler has the following modes of operation:

1. The scrambler advances and is XORed with the data.
2. The scrambler advances and is bypassed (not XORed with the data).
3. The scrambler does not advance and is bypassed (not XORed with the data).

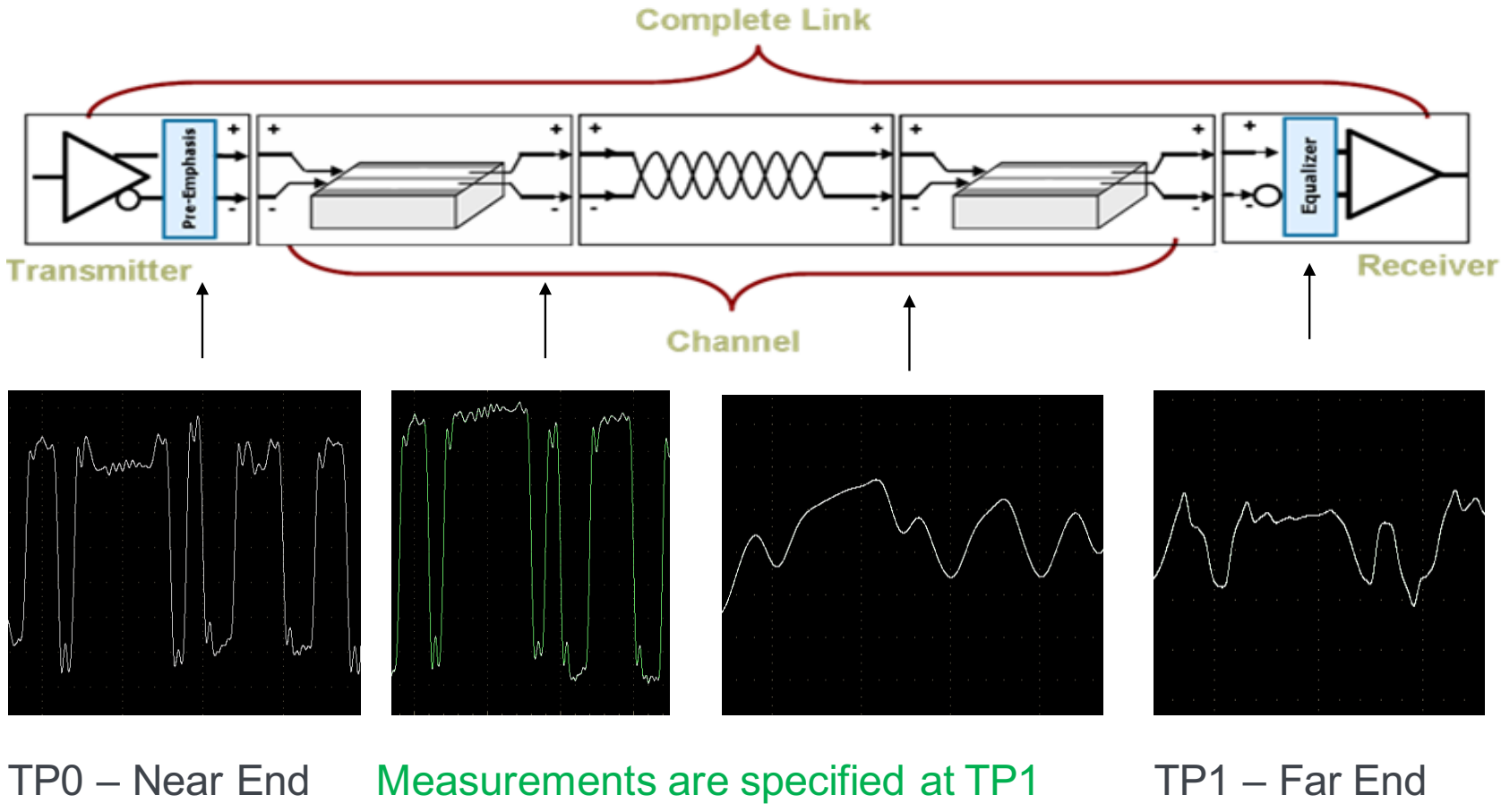
NORMATIVE 128b/132b DECODE RULES

The physical layer shall encode the data on a per block basis. Each block shall comprise a 4-bit Block Header and a 128-bit payload. The 4-bit header is set to 0011b for data and 1100b for control blocks. This header format allows for the correction of single bit errors in the header information.

Ordered sets are control blocks, and all data is sent in data blocks. The following is a list of the control blocks.

- TS1 Ordered Set
- TS2 Ordered Set
- TSEQ Ordered Set
- SYNC Ordered Set
- SKP Ordered Set
- SDS Ordered Set

End-to-End PHY Validation

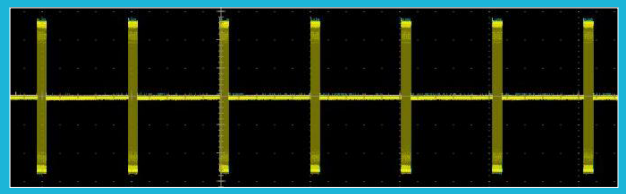


The picture above demonstrates how the signal degrades over a lossy channel when it travels from a transmitter to a receiver. This provides a perspective to the user that the eye at the receiver is likely closed and they need to implement a receiver with CTLE and DFE to open the eye.

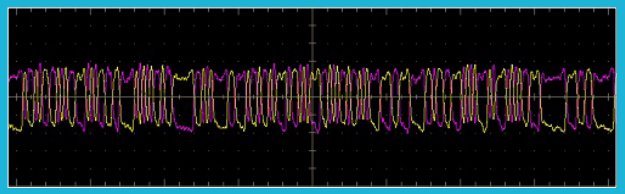
Also many high speed serial standards specify the compliance test points at the pins which is TP0. **For USB, the compliance test is specified at TP1, which is the far end, close to the receiver.**

Compliance Patterns

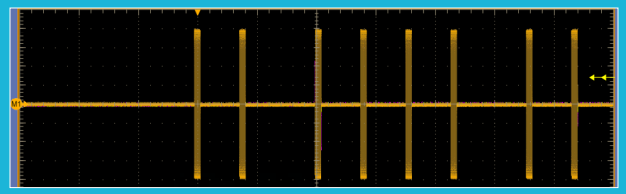
LFPS SINGLE GEN 1



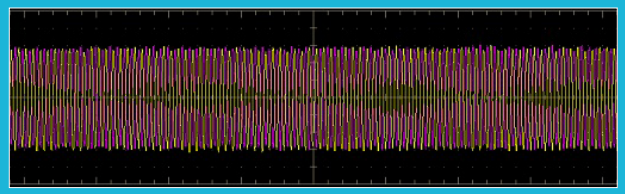
CP9



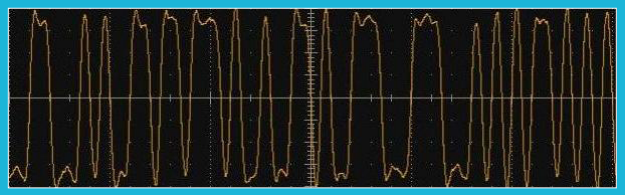
LFPS PLUS GEN 2



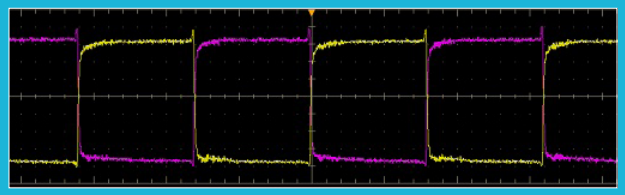
CP10



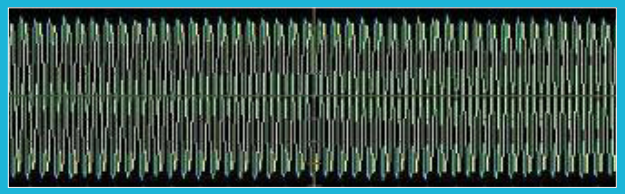
CP0



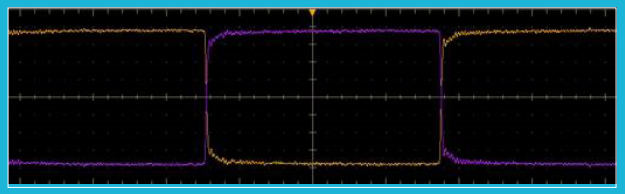
CP13



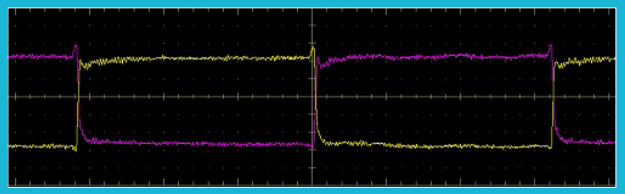
CP1



CP14



CP15



During the testing process the DUT (device under test) sometimes skips a pattern or toggles the patterns twice leading to a wrong pattern being tested. Visually it is not easy to look at the oscilloscope screen and quickly identify which pattern is being tested.

Use the screenshots below to serve as a quick reference guide for troubleshooting when the compliance test fails due to a pattern mismatch.

Print this page and place it on your bench so it is handy the next time you are testing.

Transmitter Electrical Parameters

Here are some of the critical parameters from the specification that you need to consider for your designs.

Transmitter Normative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	99.97 (min) 100.03 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations.
$\mathbf{V}_{\text{TX-DIFF-PP}}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$\mathbf{V}_{\text{TX-DIFF-PP-LOW}}$	Low-Power Differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Refer to Section 6.7.2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
$\mathbf{V}_{\text{TX-DE-RATIO}}$	Tx de-emphasis	3.0 (min) 4.0 (max)	Not applicable	dB	Nominal is 3.5 dB for Gen 1 operation. Gen 2 transmitter equalization recommendations are described in Section 6.7.5.2.
$\mathbf{R}_{\text{TX-DIFF-DC}}$	DC differential impedance	72 (min) 120 (max)	72 (min) 120 (max)	Ω	
$\mathbf{V}_{\text{TX-RCV-DETECT}}$	The amount of voltage change allowed during Receiver Detection	0.6 (max)	0.6 (max)	V	Detect voltage transition should be an increase in voltage on the pin looking at the detect signal to avoid a high impedance requirement when an “off” receiver’s input goes below ground.
$\mathbf{C}_{\text{AC-COUPLING}}$	AC Coupling Capacitor	75 (min) 200 (max)	75 (min) 265 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.
$\mathbf{t}_{\text{CDR\_SLEW\_MAX}}$	Maximum slew rate	10	Not applicable	ms/s	This is a df/ft specification; refer to Section 6.5.4 for details.
$\mathbf{SSC}_{\text{dfdt}}$	SSC df/dt	Not applicable	1250 (max)	ppm/ µs	See note 1.

Note 1. Measured over a 0.5µs interval using CP10. The measurements shall be low pass filtered using a filter with 3 dB cutoff frequency that is 60 times the modulation rate. The filter stopband rejection shall be greater or equal to a second order low-pass of 20 dB per decade. Evaluation of the maximum df/dt is achieved by inspection of the lowpass filtered waveform.

Souce: USB-IF

Transmitter Electrical Parameters (continued)

Here are some of the critical parameters from the specification that you need to consider for your designs.

Transmitter Informative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$t_{MIN-PULSE-Dj}$	Deterministic min pulse	0.96	0.96	UI	Tx pulse width variation that is deterministic
$t_{MIN-PULSE-Tj}$	Tx min pulse	0.90	0.90	UI	Min Tx pulse at 10^{-12} including Dj and Rj
t_{TX-EYE}	Transmitter Eye	0.625 (min)	0.646 (min)	UI	Includes all jitter sources
$t_{TX-DJ-DD}$	Tx deterministic jitter	0.205 (max)	0.170 (max)	UI	Deterministic jitter only assuming the Dual Dirac distribution
$C_{TX-PARASITIC}$	Tx input capacitance for return loss	1.25 (max)	1.1 (max)	pf	Parasitic capacitance to ground
R_{TX-DC}	Transmitter DC common mode impedance	18 (min) 30 (max)	18 (min) 30 (max)	Ω	DC impedance limits to guarantee Receiver detect behavior. Measured with respect to AC ground over a voltage of 0-500 mV.
$I_{TX-SHORT}$	Transmitter shortcircuit current limit	60 (max)	60 (max)	mA	The total current Transmitter can supply when shorted to ground.
$V_{TX-DC-CM}$	Transmitter DC common-mode voltage	0 (min) 2.2 (max)	0 (min) 2.2 (max)	V	The instantaneous allowed DC common-mode voltages at the connector side of the AC coupling capacitors.
$V_{TX-CM-AC-PP\_ACTIVE}$	Tx AC common mode voltage active	100	100 (max)	mVp-p	Maximum mismatch from Txp + Txn for both time and amplitude.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute DC Common Mode Voltage between U1 and U0	200 (max)	200 (max)	mV	
$V_{TX-IDLE-DIFF-AC-pp}$	Electrical Idle Differential Peak – Peak Output Voltage	0 (min) 10 (max)	0 (min) 10 (max)	mV	
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Output Voltage	0 (min) 10 (max)	0 (min) 10 (max)	mV	Voltage shall be low pass filtered to remove any AC component. This limits the common mode error when resuming U1 to U0.

Receiver Electrical Parameters

Here are some of the critical parameters from the specification that you need to consider for your designs.

Receiver Normative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	99.97 (min) 100.03 (max)	ps	UI does not account for SSC caused variations.
R_{RX-DC}	Receiver DC common mode impedance	18 (min) 30 (max)	18 (min) 30 (max)	Ω	DC impedance limits are needed to guarantee Receiver detect. Measured with respect to ground over a voltage of 500 mV maximum.
$R_{RX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	72 (min) 120 (max)	Ω	
$Z_{RX-HIGH-IMP-DC-POS}$ [1]	DC Input CM Input Impedance for V>0 during Reset or power down	25k (min)	25k (min)	Ω	Rx DC CM impedance with the Rx terminations not powered, measured over the range 0 – 500 mV with respect to ground.
$V_{RX-LFPS-DET-DIFFp-p}$	LFPS Detect Threshold	100 (min) 300 (max)	100 (min) 300 (max)	mV	Below the minimum is noise. Must wake up above the maximum.

Note 1. Only DC Input CM Input Impedance for V >0 is specified. DC Input CM Input Impedance for V <0 is not guaranteed and could be as low as 0 Ω.

Receiver Informative Electrical Parameters

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Comments
$V_{RX-DIFF-PP-POST-EQ}$	Differential Rx peak-to-peak voltage	30 (min)	30 (min)	mV	Measured after the Rx EQ function (Section 6.8.2).
t_{RX-TJ}	Max Rx inherent timing error	0.45 (max)	0.394 (max)	UI	Measured after the Rx EQ function (Section 6.8.2).
$t_{RX-DJ-DD}$	Max Rx inherent deterministic timing error	0.285 (max)	0.21 (max)	UI	Maximum Rx inherent deterministic timing error.
$C_{RX-PARASITIC}$	Rx input capacitance for return loss	1.1 (max)	1.0 (max)	pF	
$V_{RX-CM-AC-P}$	Rx AC common mode voltage	150 (max)	150 (max)	mV Peak	Measured at Rx pins into a pair of 50 Ω terminations into ground. Includes Tx and channel conversion, AC range up to 5 GHz
$V_{RX-CM-DC-ACTIVE-IDLE-DELTA\_P}$	Rx AC common mode voltage during the U1 to U0 transition	200 (max)	200 (max)	mV Peak	Measured at Rx pins into a pair of 50 Ω terminations into ground. Includes Tx and channel conversion, AC range up to 5 GHz

Normative Receiver Tolerance Compliance Test Parameters

Here are some of the critical parameters from the specification that you need to consider for your designs.

Input Jitter Requirements for Rx Tolerance Testing

Symbol	Parameter	Gen 1 (5.0 GT/s)	Gen 2 (10 GT/s)	Units	Notes
f1	Tolerance corner	4.9	7.5	MHz	
J_{Rj}	Random Jitter	0.0121	0.01308	UI rms	1
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	0.184	UI p-p	1,4
J_{Pj_500kHz}	Sinusoidal Jitter	2	4.76	UI p-p	1,2,3
J_{Pj_1MHz}	Sinusoidal Jitter	1	2.03	UI p-p	1,2,3
J_{Pj_2MHz}	Sinusoidal Jitter	0.5	0.87	UI p-p	1,2,3
J_{Pj_4MHz}	Sinusoidal Jitter	N/A	0.37	UI p-p	1,2,3
J_{Pj_f1}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_50MHz}	Sinusoidal Jitter	0.2	0.17	UI p-p	1,2,3
J_{Pj_100MHz}	Sinusoidal Jitter	N/A	0.17	UI p-p	1,2,3
V_full_swing	Transition bit differential voltage swing	0.75	0.8	V p-p	1
V_EQ_level	Non transition bit voltage (equalization)	-3	Preshoot = 2.7 De-emphasis = -3.3	dB	1

Notes:
1. All parameters measured at TP1.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Random jitter is also present during the Rx tolerance test.
5. The JTOL specs for Gen 2 comprehend jitter peaking with re-timers in the system and has a 25dB/decade slope.

LFPS Transmitter Electrical Specifications and Timing for SuperSpeed Designs

Here are some of the critical parameters from the specification that you need to consider for your designs.

Normative LFPS Electrical Specification

Symbol	Minimum	Typical	Maximum	Units	Comments
tPeriod	20		100	ns	
tPeriod for SuperSpeedPlus	20		80	ns	
$V_{CM-AC-LFPS}$			$V_{TX-CM-AC-PP-ACTIVE}$	mV	See Table 6-18 in the complete USB 3.1 specifications rev 1.0 July 23, 2013.
$V_{CM-LFPS-Active}$			10	mV	
$V_{TX-DIFF-PP-LFPS}$	800		1200	mV	Peak-peak differential amplitude
$V_{TX-DIFF-PP-LFPS-LP}$	400		600	mV	Low power peak-peak differential amplitude
tRiseFall2080			4	ns	Measured at compliance TP1, as shown in Figure 6-19 in the complete USB 3.1 specifications rev 1.0 July 23, 2013.
Duty Cycle	40		60	%	Measured at compliance TP1, as shown in Figure 6-19 in the complete USB 3.1 specifications rev 1.0 July 23, 2013.

LFPS Transmitter Electrical Specifications and Timing for SuperSpeed Designs (continued)

LFPS Transmitter Timing for SuperSpeed Designs[1]

	tBurst				tRepeat		
	Minimum	Typical	Maximum	Minimum Number of LFPS Cycles [2]	Minimum	Typical	Maximum
Polling.LFPS	0.6 µs	1.0 µs	1.4 µs		6 µs	10 µs	14 µs
Ping.LFPS[8]	40 ns		200 ns	2	160ms	200ms	240ms
Ping.LFPS for SuperSpeedPlus[9]	40 ns		160 ns	2			
tReset[3]	80 ms	100ms	120 ms				
U1 Exit[4,5]	600 ns[7]		2 ms				
U2/Loopback Exit[4,5]	80 µs[7]		2 ms				
U3 Wakeup[4,5]	80 µs[7]		10 ms				

Notes:
1. If the transmission of an LFPS signal does not meet the specification, the receiver behavior is undefined.
2. Only Ping.LFPS has a requirement for minimum number of LFPS cycles.
3. The declaration of Ping.LFPS depends on only the Ping.LFPS burst.
4. Warm Reset, U1/U2/Loopback Exit, and U3 Wakeup are all single burst LFPS signals. tRepeat is not applicable.
5. The minimum duration of an LFPS burst shall be transmitted as specified. The LFPS handshake process and timing are defined in Section 6.9.2 of the complete USB 3.1 specifications rev 1.0 July 23, 2013.
6. A Port in U2 or U3 is not required to keep its transmitter DC common mode voltage. When a port begins U2 exit or U3 wakeup, it may start sending LFPS signal while establishing its transmitter DC common mode voltage. To make sure its link partner receives a proper LFPS signal, a minimum of 80 µs tBurst shall be transmitted. The same consideration also applies to a port receiving LFPS U2 exit or U3 wakeup signal.
7. A port is still required to detect U1 LFPS exit signal at a minimum of 300ns. The extra 300ns is provided as the guard band for successful U1 LFPS exit handshake.
8. This requirement applies to SuperSpeed only designs (are only capable of operating at 5Gb/s).
9. This requirement applies to SuperSpeedPlus designs (capable of operating at 10Gb/s and higher speeds).

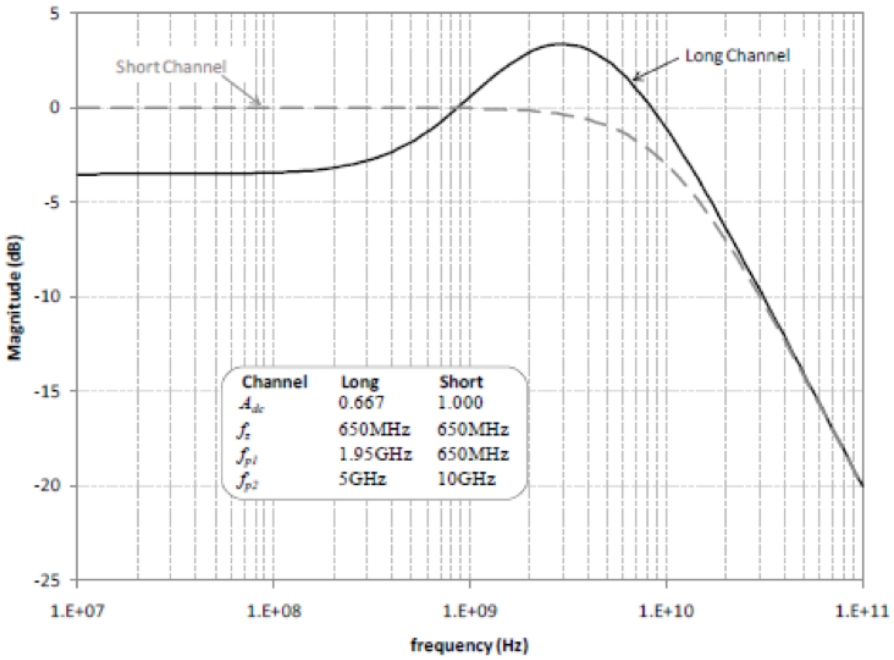
Gen 1 Reference CTLE

USB 3.1 allows the use of receiver equalization to meet system timing and voltage margins. For long cables and channels the eye at the Rx is closed, and there is no meaningful eye without first applying an equalization function. The Rx equalizer may be required to adapt to different channel losses using the Rx EQ training period. The exact Rx equalizer and training method is implementation specific.

The equation for the Continuous Time Linear Equalizer (CTLE) used to develop the specification is the compliance Rx EQ transfer function described below.

$$H(s) = \frac{A_{dc}\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

where A_{dc} is the DC gain
$\omega_z = 2\pi f_z$ is the zero frequency
$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency
$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency

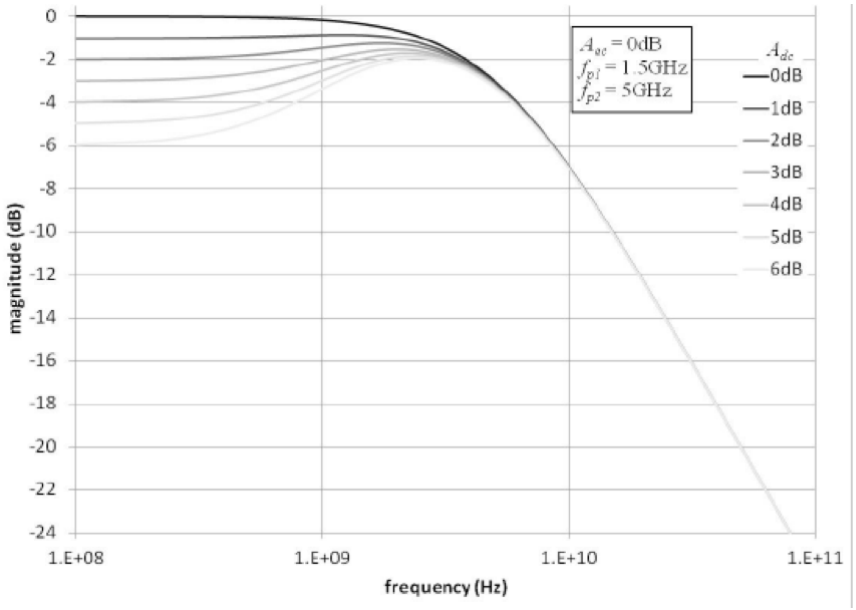


Gen 2 Reference Equalizer Function

Equation below describes the frequency response for the Gen 2 Reference Continuous Time Linear Equalizer (CTLE) that is used for compliance testing. The equation describes the same first order CTLE as contained in equation for Gen 1

$$H(s) = A_{ac}\omega_{p2}\frac{s + \frac{A_{dc}}{A_{ac}}\omega_{p1}}{(s+\omega_{p1})(s+\omega_{p2})}$$

where A_{ac} is the high frequency peak gain
A_{dc} is the DC gain
$\omega_{p1} = 2\pi f_{p1}$ is the first pole frequency
$\omega_{p2} = 2\pi f_{p2}$ is the second pole frequency

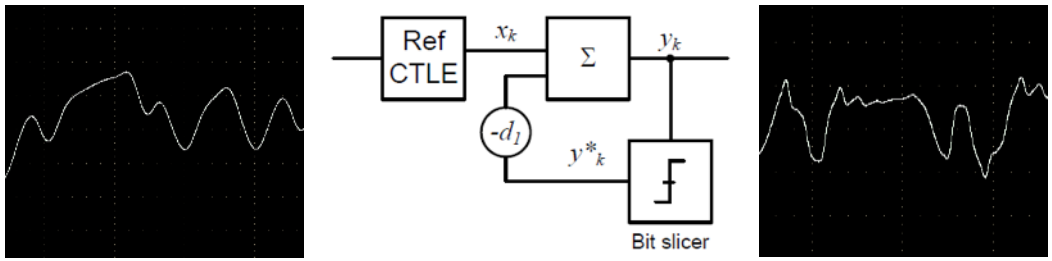


Reference DFE

In addition to the 1st order CTLE, a one-tap reference DFE is used in transmitter compliance testing. The DFE behavior is described by the equation and Figure below. The limits on d_1 are 0 to 50mV.

$$y_k = x_k - d_1\,\mathrm{sgn}(y_{k-1})$$

where y_k is the DFE differential output voltage
y^*_k is the decision function output voltage, $|y^*_k| = 1$
x_k is the DFE differential input voltage
d_1 is the DFE feedback coefficient
k is the sample index in UI



Initiating Loopback - Power On Device

GEN 1

4 msec

To get the DUT into loopback, the BERT sends pattern sequences and the device under test (DUT) needs to respond to these sequences for a successful loopback. Once the loopback is successful, JTOL testing can begin.

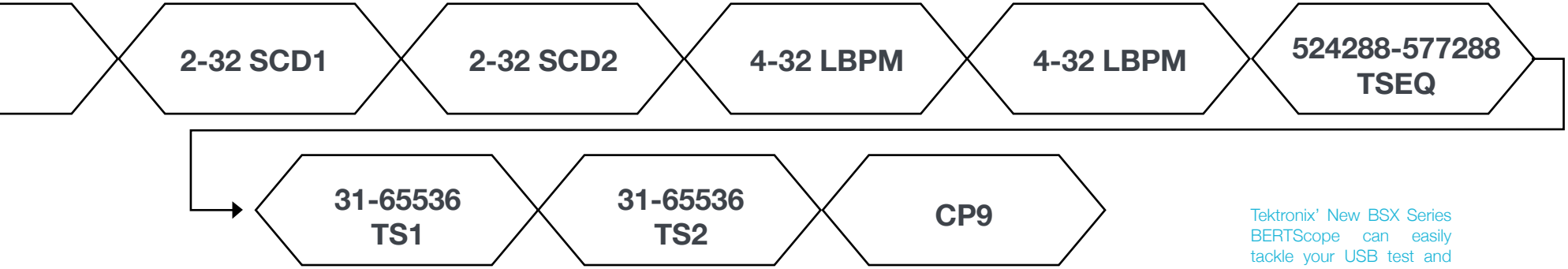
Gen 1 Loopback Sequence:

- **Transmit 400 Polling.LFPS (4 msec).**
- **Transmit 65536 TSEQ.**
- **Transmit 256-65536 TS1.**
- **Transmit 256-65536 TS2 with loopback bit set.**
- **Start transmitting the BDAT test pattern for 2 msec before starting error calculations.**

Note that all jitter sources are added during all transmissions to the device under test. If the device does not go into loopback it fails the test.

Initiating Loopback - Power On Device

GEN 2



Gen 2 Loopback Sequence:

» **LFPS/LFPS Plus:**
- 2-32 SCD1
- 2-32 SCD2
- 4-32 LBPM (w PHY capability)
- 4-32 LBPM (w PHY ready)

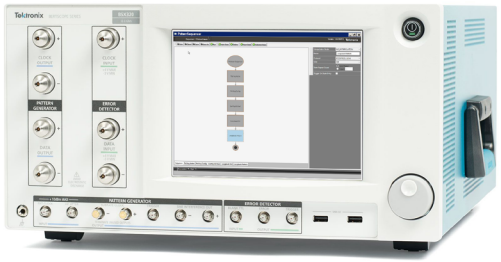
» **524,288 - 577,288 TSEQ It is preferred for the BERT to transmit as close to 524,288 TSEQ as possible**

» **31 - 65536 TS1 (SYNC, 31 TS1, SKP - repeat to up to 65536 total TS1)**

» **31 - 65536 TS2 with loopback bit set**

» **Start transmitting the CP9 test pattern. Transmit CP9 for 2 msec before starting error calculations.**

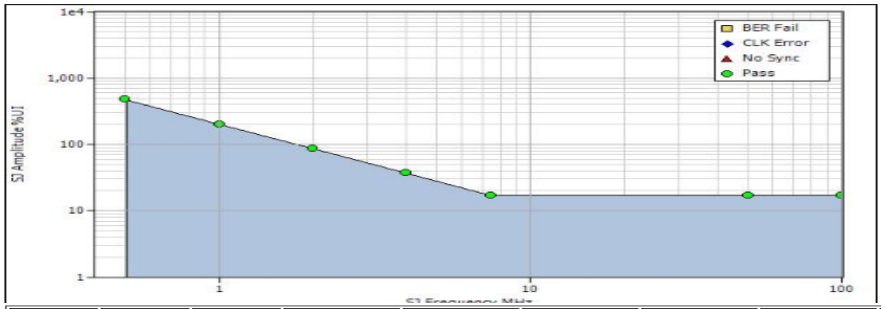
Note that all jitter sources are added during all transmissions to the device under test. If the device does not go into loopback it fails the test.



Receiver Tolerance Test Overview (JTOL)

- 8 test points for USB 3.1 Gen 1 and 9 test points USB 3.1 Gen2
- SSC Clocking is enabled
- BER Test is performed at 10^{-10} for USB 3.1 Gen 1
- For Gen 2 - BER Test is performed at each Sj tone for 2 mins
- Preshoot/De-emphasis enabled
- Stress verified by TJ/Eye Height
- Each SJ term in the table is tested one at a time after the device is in loopback mode

The only test the user needs to perform for receiver compliance testing is JTOL. The above high level bullets are important to remember when you are running jitter tolerance test. Failure to set these right parameters can lead to being non-compliant and failure of test.



MHZ	Test	Template	Bits	Errors	BER	Status	Margin
0.50	476.00%	476.00%	3.00e010	0	0.00e000	Passed	0.00%
1.00	203.00%	203.00%	3.00e010	0	0.00e000	Passed	0.00%
2.00	87.00%	87.00%	3.00e010	0	0.00e000	Passed	0.00%
4.00	37.00%	37.00%	3.00e010	0	0.00e000	Passed	0.00%
7.50	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
50.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
100.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%

GEN 1 JTOL TABLE

Frequency	SJ	RJ
500 kHz	400ps	2.42ps RMS
1 MHz	200ps	2.42ps RMS
2 MHz	100ps	2.42ps RMS
4.9 MHz	40ps	2.42ps RMS
10 MHz	40ps	2.42ps RMS
20 MHz	40ps	2.42ps RMS
33 MHz	40ps	2.42ps RMS
50 MHz	40ps	2.42ps RMS

GEN 2 JTOL TABLE

Frequency	SJ	RJ
500kHz	476ps	1.308ps RMS
1MHz	203ps	1.308ps RMS
2MHz	87ps	1.308ps RMS
4MHz	37ps	1.308ps RMS
7.5MHz	17ps	1.308ps RMS
15MHz	17ps	1.308ps RMS
30MHz	17ps	1.308ps RMS
50MHz	17ps	1.308ps RMS
100MHz	17ps	1.308ps RMS

Challenges of TX Testing for Type-C Devices

FROM COMPLEXITY TO CONFIDENCE

Beyond Compliance

Only relying on compliance tests is not sufficient when you are working on characterizing and margining your parts. You need standard specific measurements built into the oscilloscope along with analysis tools such as vertical and horizontal jitter decomposition to understand device behaviors.

To build confidence on the margin on your devices, you need the ability to render an eye diagram with extrapolation using BER contours and analyze the channel effect on the signal at the far end.

When a device fails a compliance test, you need the ability to load those same measurements on the scope, gate them using cursors along with visual search capabilities.

Tektronix' DPOJET and SDLA are the analysis and debugging tools, which help accomplish testing beyond compliance.

Reduce Validation Time

Test times always play a vital role when access to the DUT is limited. As designs mature and move to manufacturing, even 5 mins of savings on a production floor translates to huge ROI.

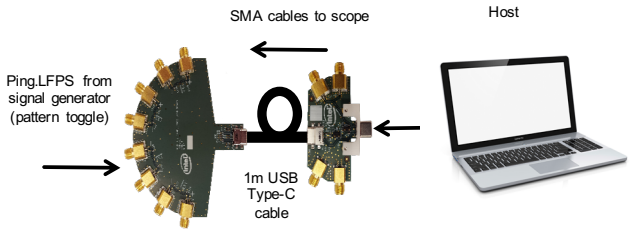
Ability to run these measurements using python scripts and being able to easily integrate them into the bigger automation environment is vital. This reduces a lot of manual intervention of the tests, simplifying the validation process and improves productivity of the team.

With Tektronix' solution you can finish both USB Gen 1 and Gen 2 test suites in less than 20 minutes.

Global Collaboration

Collaborating with global teams can be challenging especially when there isn't an easy way to share and analyze waveforms. This wastes time, energy and can be quite frustrating.

Easily collaborate more efficiently with co-workers, suppliers and customers worldwide with Tektronix' solution. You can analyze waveforms in an offline mode, send them to the necessary people and then work together remotely to solve design issues.



Challenges of RX Testing for Type-C Devices

FROM COMPLEXITY TO CONFIDENCE

Protocol Awareness

With the complexity of the USB specifications, it is hard to track down where in the loopback sequence does your device under test fail. You need the ability to visually look at the pattern sequence trace being sent by the BERT to the DUT and understand which part of the sequence is not being looped back.

Having protocol awareness built into the BERTScope enables the user to troubleshoot loopback sequence issues and provides insight in terms of timing issues or pattern sequence being non-compliant.

Debug

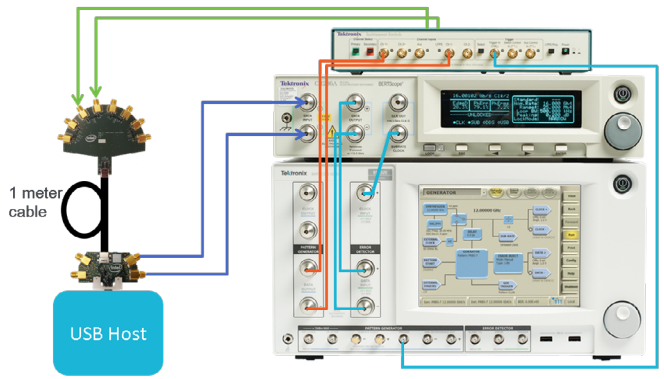
When compliance testing fails it is time consuming to find the root cause. The ability to see some trends in failures to derive conclusions is vital.

The fastest and easiest way is to have sophisticated error analysis tools at your disposal. **The bit-error location tool on Tektronix' BERTScope provides insight on the randomness or systematic behavior of errors being reported during JTOL test. This allows you to isolate the issues, be it on the design side or due to channel effects.**

Beyond Compliance

Receivers can be expensive to design and over designing margins on the Receiver can be even more expensive. To ensure that the Receiver has sufficient margin to pass compliance, be competitive while maintaining the cost of the parts can be a tricky affair.

Margin analysis tools on the BERTScope helps you understand the margin available on early designs and make the right kind of trade off decisions before you finalize your designs. The ability to test beyond compliance with such margin tools makes the difference for your product to be a winner in market place.



Tektronix' New BSX Series BERTScope can easily tackle your USB test and measurement challenges.

Key Considerations

Things to think about before planning your USB testing and certification for compliance:

- **How will you get more insight into measurements failures reported by SigTest for characterization?**
- **How will you execute SSC measurements, which are not available in SigTest for Gen 1 Testing?**
- **How will you ensure that your device interoperability is within the compliance limits for last 3 generations of USB Spec?**
- **How will you manage to test beyond the compliance test limits for margin analysis?**
- **How will you test at the far end and simulate the receiver adaptation for different DFE values?**
- **How will you automate all the measurements to reduce test times?**
- **How will you ensure that your device will be certified by USBIF?**
- **How do you plan to resolve loopback initialization challenges?**
- **How do you plan to debug issues when your DUT fails JTOL test?**
- **How do you plan to build competitive specifications for your products, which highlight margins on your products?**

Don't waste your time.
Make sure your device passes the first time.

Ensure you partner with a certified and approved vendor for the USBIF so you have the confidence your design will pass compliance testing. Visit one of Tektronix' suites at the next plugfest:

- USB 3.1 Gen2 Tx & Rx – USBIF Approved Gold Test Suite
- USB 3.1 Gen1 Tx & Rx – USBIF Approved Gold Test Suite
- USB 2.0 – USBIF Approved Gold Test Suite
- USB PD – USBIF Approved Gold Test Suite

Need help in answering these questions.
Your Tektronix Account Manager will be happy to help, just give them a call.

To contact any of our worldwide offices for assistance please refer to the telephone numbers on the next page.

Reference URLs:

USB3.1 Base spec and supplemental specs
http://www.usb.org/developers/docs/

USB Type-C cable and connector specification
http://www.usb.org/developers/usbtypec/

Compliance Test Specification (CTS)
http://www.usb.org/developers/compliance/ssusb_testing/

Tektronix USB3.1 solution, MOIs, Webinars, Application Notes:
https://www.tek.com/usb

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Find more valuable resources at TEK.COM

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